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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,149	02/14/2002	Milivoje Aleksic	00100.02.0060(990060D-1)	7928

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ATI TECHNOLOGIES, INC.
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EXAMINER
KING, JUSTIN

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,149	ALEKSIC ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 24 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended claim 24 recites a data storage coupled to the I/O controller via a second high speed bus. The amended limitation is not disclosed or supported by the original Specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 18-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Iachetta, Jr. (U.S. Patent No. 5,727,171), Porterfield (U.S. Patent No. 6,141,715), Ajanovic et al. (U.S. Patent No. 5,859,988), and Heil et al. (U.S. Patent No. 5,392,407).

Referring to claims 18 and 22: Iachetta discloses a data processing system including a system controller (figure 4, structure 640) and an I/O controller (figure 4, structure 810). Iachetta discloses a memory system (figure 4, structure 660) connected to the system controller. Although Iachetta does not explicitly disclose the logic for controlling the memory's I/O operations, Iachetta's memory cannot function properly without one. Such memory I/O control logic is the claimed memory control channel. Iachetta discloses that the system controller connects to a high-speed PCI bus (figure 4, structure 680), and the I/O controller connects to a low-speed PCI bus (figure 4, structure 860).

Although Iachetta does disclose a high-speed arbiter (figure 4, structure 710) for the high-speed bus and a low-speed arbiter (figure 4, structure 910) for the low speed bus, Iachetta does not disclose that the I/O controller coupled to the high-speed arbiter via the high-speed bus, and Iachetta does not disclose that the arbiter is an integrated part of the controllers. Iachetta also does not disclose two separate memory channel controllers.

Porterfield discloses a system controller (figure 2, structure 16) with an integrated arbiter (figure 2, structure 42). Porterfield discloses that the PCI devices connect to the integrated arbiter via the PCI bus (figure 2, structure 20). Since each bus bridge creates a new bus segment, an arbitration function is an anticipated common bridge feature. Porterfield teaches one to avoid

live lock condition on the computer bus with a system controller and an integrated arbiter (abstract). Porterfield teaches one to equip the bridge an arbiter to resolve the live lock condition.

Ajanovic discloses an I/O controller (figure 3, structure 205) with an integrated arbiter (figure 3, structure 308). Ajanovic teaches one to improve the system performance by centralize the bus request arbitration with dedicated buffers (figure 3, structures 304-306) for each bus segment.

Heil discloses a multiple-port structure. Heil discloses two separate memory channel controllers (figure 8, structures 134, 136, 142, and 144). Heil teaches that the general access latency caused by the severe bandwidth constraint can be improved with the dual memory channels (column 1, lines 52-56).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Porterfield, Ajanovic, and Heil's teachings onto Iachetta because Porterfield teaches one to equip the bridge an arbiter to resolve the live lock condition, Ajanovic teaches one to improve the system performance by centralize the bus request arbitration with dedicated buffers, and Heil teaches one to improve the general access latency by the dual memory channels.

Referring to claims 19-20: Iachetta's high-speed bus at 66 MHz is at least 10 percent faster than the low-speed bus at 33 MHz.

Referring to claim 23: Iachetta discloses an I/O device (figure 4, structure 940) coupled to the control circuitry of the second controller (figure 4, structure 810) without being coupled to the arbiter of the first controller (figure 4, structure 640).

6. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Iachetta and Kelley et al. (U.S. Patent No. 6,295,568).

Referring to claim 22: Iachetta discloses a data processing system including a system controller and a first arbiter (figure 4, structures 640 and 710), and an I/O controller and a second arbiter (figure 4, structures of 810 and 910). Iachetta discloses that the system controller connects to a high-speed PCI bus (figure 4, structure 680), and the I/O controller connects to a low-speed PCI bus (figure 4, structure 860). The high-speed PCI bus is the claimed first bus of a predefined protocol type at a first data rate. The low-speed PCI bus is the claimed second bus. The I/O controller's connecting means to the high-speed PCI bus is the claimed control circuitry. Iachetta does not disclose that each arbiter is physically integrated into the system controller or the I/O controller.

Kelly discloses a bridge supporting multiple frequency speeds (figure 3). Kelly's bridge has an integrated arbiter (figure 3, structure 102) to arbitrate bus access among different frequency segments. Kelly teaches one to integrate the arbiter into the bridge to arbitrate the bus according to the priority.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Kelly's teachings onto Iachetta because Kelly teaches one to integrate an arbiter into the bridge to arbitrate the bus according to the each frequency segment's relative workload.

Referring to claim 23: Iachetta discloses an I/O device (figure 4, structure 940) couple to the control circuitry of the second controller without being coupled to the arbiter of the first controller.

Response to Arguments

7. In response to Applicant's arguments and amendment: The Office Action above has been revised to reflect the claim amendment.

Conclusion

8. The prior art made of recorded previously and not relied upon is considered pertinent to applicant's disclosure.

PCI-to-PCI Bridge Architecture Specification, Section 8.2: The Specification explicitly discloses that it is anticipated that an arbiter is a common bridge feature.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
May 12, 2006

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